Memory Merchant™

IEEE 696/S-100

MM65K16S

64K STATIC RAM

USER'S MANUAL

(REV 3)

14666 DOOLITTLE DR. SAN LEANDRO, CA. 94577 (415) 483-1008

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* CROMIX and CDOS are trademarks of Cromemco Inc.
† MP/M is a trademark of Digital Research

1. INTRODUCTION

Thank you for choosing the Memory Merchant Model MM65K16S. You have purchased one of the most versatile 64K Static S-100 memory boards available on the market today. Using complex programmable logic arrays, we were able to design a memory board with incredible features such as:

BANK SELECT–
The bank select feature is switch setable to any one of 256 available I/O addresses and will respond to any one or combination of the eight data bits that are desired.

EXTENDED ADDRESSING–
Extended addressing allows the MM65K16S to reside anywhere in the memory map with no imposed limitations by the addressing range of the microcomputer system.

2K SEGMENT DISABLE–
The MM65K16S is capable of disabling a 2K segment of memory anywhere in the memory map. This feature is necessary in systems that include a memory mapped disk controller or video display interface.

CROMEMCO COMPATIBLE–
This board has been field tested in Cromemco CDOS* and CROMIX* systems. The MM65K16S is completely compatible with CROMIX* bank select type software without the need for an additional chip set or any modification to the board while allowing CROMIX* to run in excess of 6.5 Mhz. (without phantom)

PHANTOM–
The memory is organized as two independent 32K banks. Each 32K bank individually responds to the phantom line.

SPEED–
The MM65K16S is guaranteed to run with any 8 bit 8080, Z80 or 8085 processor on the market today. In fact, the MM65K16S is guaranteed to run reliably with processors that have clock speeds in excess of 6Mhz (without phantom).

POWER–
The MM65K16S draws an average of 500 ma. of current with code executing in ram (64K) along with sufficient on-board regulation to enable the user to load the board completely with Eprom.

2. OVERVIEW

We have taken great care in assembling this new manual. A lot of thought went into making this manual more helpful and easier to understand for our customers. We have added the following new pages:

* SPECIFICATIONS
* EXPANDED BOARD LAYOUT
* HOW THE BOARD IS SHPPPED
* BOARD PURCHASES AS A 48K/32K
* INSERTING/REMOVING IC'S
* USING EPROMS/BIPOLAR PROMS
* OPTION #A48/16
* FULL CROMIX* INSTRUCTIONS
* IF YOUR BOARD FAILS TO OPERATE!

Along with these new sections, we have added a variety of tables and new pictures that will enable you to instantly know how the switches are set. We believe that anyone who carefully reads this manual will understand, with little or no difficulty, how to operate the MM65K16S.

Pay close attention to the board layout on page 5. This shows the board and underneath a picture of the memory addressing switch (5D) and how it is physically tied to the BANKS, BLOCKS, PHANTOM Lines, ENABLE/DISABLE headers (J6,6,5,4) and 2K segment disable block Ø. This picture gives and overview and makes it easier to understand once you have read the separate sections on the different functions of the board in "6. Installation Instructions".

We welcome any comments you wish to make concerning this new manual. You can write to Memory Merchant Attn: Greg Besse

Limited Warranty

Memory Merchant warrants its products to be free from defects in workmanship and materials for a period of 18 months from the date of shipment/Invoice from Memory Merchant of Dealer/Agent to the original end user. If any memory board becomes defective within the first six (6) months from the date of shipment/Invoice, Memory Merchant will replace, not repair, that unit. Should any memory board become defective after the initial six (6) month warranty period, Memory Merchant reserves the right to replace or repair that unit which proves to be defective. The warranty is Void if, in the sole opinion of Memory Merchant, the product has been subject to abuse, misuse, unauthorized modification, Serial No. modification, or if the unit is used in any other manner than intended. All warranties are non-transferable and are Void if any Memory Merchant product is sold by the original end user to any other end user.

Return Policy:

1) All defective products in question, whether purchased directly from Memory Merchant or through a Dealer/Agent, must be returned to Memory Merchant for repair or replacement according to the condtions set forth in the above warranty.
2. Prior to shipping any defective product for replacement or repair, you must receive a Return Material Authorization (RMA) number from Memory Merchant. When requesting an RMA No., please provide the following information: A description of the problem with as much detail as possible; Serial No. (s) of the unit (s); where the unit was purchased along with the date of purchase.
3) Upon receiving an RMA No. from Memory Merchant, pack the unit (s) along with a copy of your proof of purchase and ship it prepaid to Memory Merchant. Items received without proof of purchase will be returned at senders expense. The RMA No. MUST BE MARKED on the OUTSIDE of the shipping container or it will be refused.
4) Repaired or replacement products, still in warranty, will be shipped prepaid by UPS Surface. Customer requests for any method of shipment other than UPS Surface will be chargeable to the Customer. All requests for Air Freight will be shipped Collect.
5) All out of warranty products returned for repair or testing will be assessed a minimum of $50.00 service charge. If the charge for repair is to exceed $50.00, the customer will be notified (For Authorization) prior to starting the actual repair. An RMA No. is required for out-of-warranty returns!

The foregoing warranty is in lieu of all other warranties either expressed or implied and, in any event, is limited to product repair or replacement.

Effective 11/1/81

All prices, Terms, Specifications are subject to change without notice.

4. SPECIFICATIONS FOR MODEL MM65K16S (REV 3)

A.) TESTING:

Memory Test: Run prior to and after burn-in
Burn-in Time: 96 Hrs. (4 Days) under Power (+8V)
Burn-in Temp.: 50° C
Speed: In excess of 6 Mhz. (without Phantom)

B.) POWER CONSUMPTION:

(+8V) – 64K Version = 625 ma. max.*
48K Version = 575 ma. max.*
32K Version = 525 ma. max.*

*note: The above current specs. were obtained using the Mitsubishi NMOS 16K (2K x 8) 150ns Static Ram Part No. #M58725P-15

C.) MEMORY CHIPS:

16K (2K x 8) Static Ram / 150 ns max. access time
24 Pins - .600" spacing row/row

Manufacturers Tested (MM65K16S)		*Other Manufacturers	
MITSUBISHI	#M58725P-15	FUJITSU	#MB8128
HITACHI	#HM6116P-3	TOSHIBA	#TMM2016
NEC	#UPD4016-3	OKI SEMI.	#MSM2128

*note: Although these manufacturer's pin-outs are identical to the ones tested in our boards, we have not tested nor can we guarantee that the performance will be the same.

D.) EPROMS/BIPOLAR PROMS:

Consult page 18 of the users manual

E.) SPECIAL COMPONENTS:

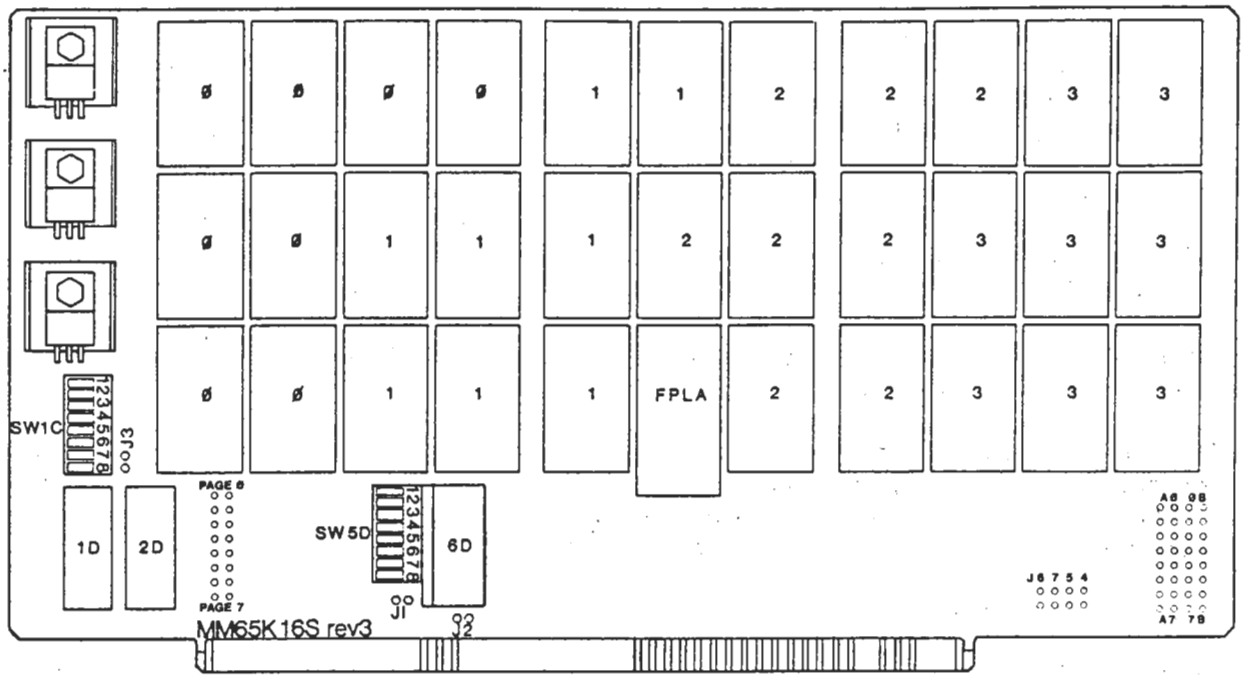
Custom programmed logic:

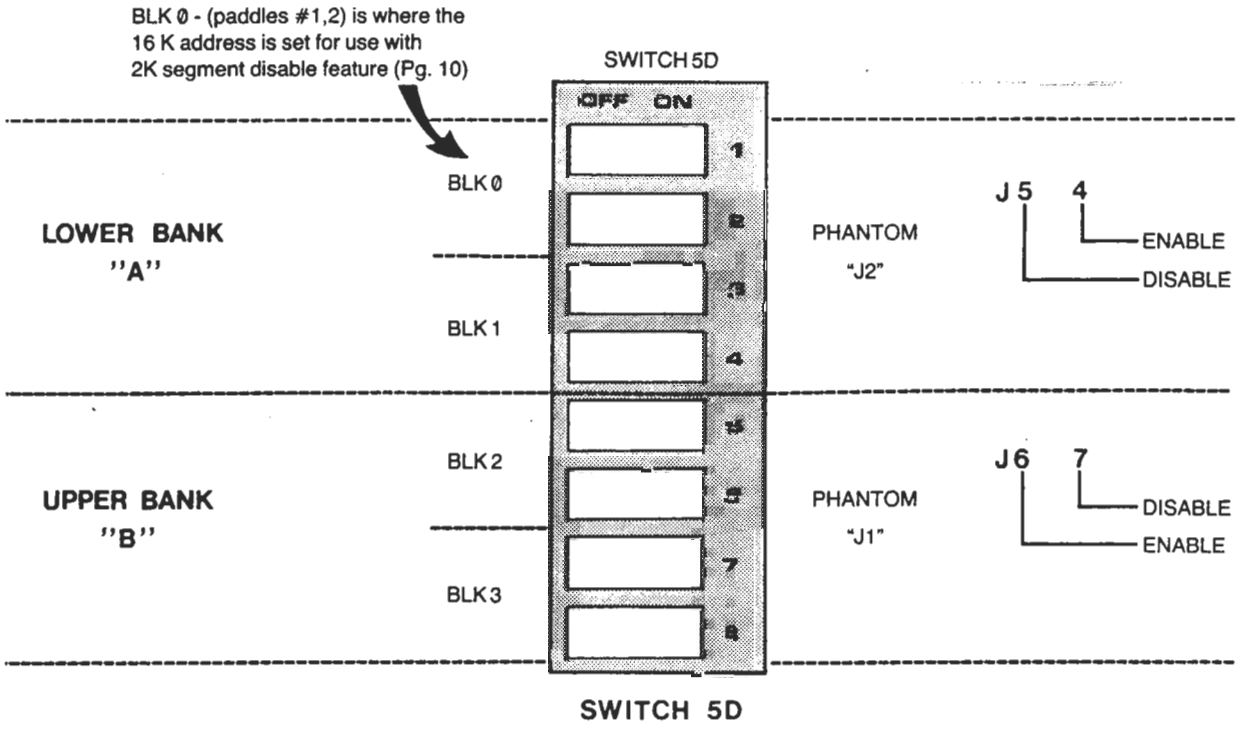
1.) PAL14L4 (IC. LOC. 6D) Programmable Array Logic
2.) PAL16L2 (IC. LOC. 16D) Programmable Array Logic
3.) 82S100 (IC. LOC. 9C) Field Programmable Logic Array

F.) OPTION #A48/16

Consult page 16 of the users manual

MM65K16S (Rev3) Component Layout





6.1. HOW THE BOARD IN SHIPPED.....

The MM65K16S is put through a variety of tests to insure that all functions work properly before shipping. Because of the many possible configurations that can be set-up with our board, we package the shunts separately rather than mounting them on the headers (on the board). Although most users do not require more than 4 to 6 shunts, we supply enough for all possible configurations - such as multiple bank switching as required for use in the Cromemco Cromix* system.

Before installing any of the shunts onto the board, please read the complete section "6. Installation Procedures". This will enable you to configure the board for your systems' requirements. Please note that the board has only two modes of operation - bank select or extended addressing. We ship the board in the bank select mode. In this mode, IC socket location 2D is populated with the 25LS2521 and dip switch 1C will be set to port 40 Hex. To complete the bank selct mode, you must install a shunt onto the header labled "J3". Header J3 is located to the immediate right of dip switch 1C.

If you just want the board to reside in the first 64K of the memory map and do not care about bank select or extended addressing, simply leave the board in the bank select mode and install a shunt on "J3". If the shunt is not placed on this header, the board will fail to start-up and run. Also, remember that at least one of the paddles, on dip switch 1C, must be in the ON postion for operation in the first 64K of the memory map.

Proper memory addressing (dip sw. 5D) and installing the balance of the shunts on the headers can only be accomplished by carefully reading all of the installation procedures and special application notes presented in this manual. By following these procedures, you will prevent start-up problems and eliminate needless and costly phone calls to the factory. If you do have problems and are sure all instructions were carefully followed - proceed to section "8. If your board fails to operate!

6. INSTALLATION PROCEDURES
6.2. ENABLES AND PHANTOM
6.2.1. ENABLE/DISABLE AT POWER ON CLEAR OR RESET

The MM65K16S memory board can be divided into two "banks" of memory that can be enabled or disabled when POWER ON CLEAR or RESET are in an active state. In order for all 64K of memory to be active on the bus both "banks" of memory must be configured to enable in response to either POWER ON CLEAR or RESET.

An 8-pin header is located under IC 15D (74LS74) and is used to set the board so that either one or both of the banks of memory will be enabled or disabled whenever RESET or POWER ON CLEAR are active on the bus. This header is labeled J6 7 5 4 and is configured by shunts that are placed across the row of pins.

The diagram below shows the jumper indications and the bank of memory that each jumper controls.

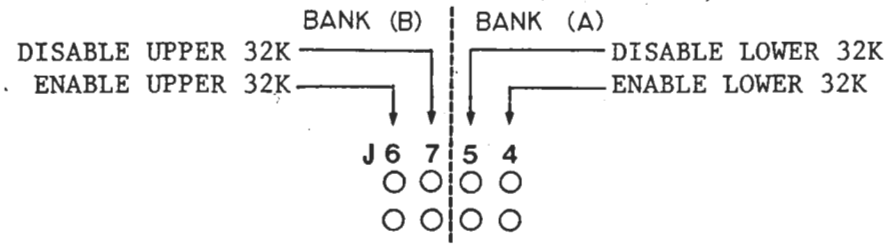
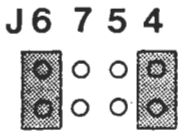


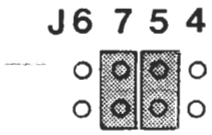
Figure 6-1: RESET AND POJ CONFIGURATION HEADER

The following examples indicate the four possible settings for the enable/disable feature.

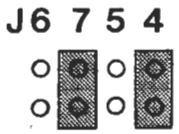
BOTH 32K BANKS ENABLED



BOTH 32K BANKS DISABLED



UPPER 32K DISABLED
LOWER 32K ENABLED



UPPER 32K ENABLED
LOWER 32K DISABLED

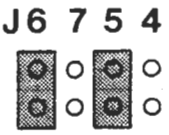


Figure 6-2: POJ AND RESET CONFIGURATIONS

CAUTION: DO NOT INSTALL SHUNT JUMPERS ACROSS (J4 AND J5) OR (J6 AND J7) AT THE SAME TIME, AS UNPREDICTABLE RESULTS COULD OCCUR.

6.2.2 PHANTOM

The PHANTOM option is used to remove a section or sections memory from the bus during specific operations. Some of these operations might include the enabling of a bootstrap loader, ROM monitor, or a POWER ON JUMP function.

Because there are two 32K banks of memory, it is necessary to configure the MM65K15S for proper operation with PHANTOM. Because both the upper and lower 32K banks of RAM individually respond to PHANTOM, it is mandatory that the MM65K16S be properly configured to recognize or ignore the PHANTOM signal.

The headers labeled J1 and J2 control PHANTOM. The J1 header is located directly below the DIP switch at 5D and controls PHANTOM for the upper 32K of memory. J2 is located directly below the IC in location 6D and controls the PHANTOM for the lower 32K of memory. As in the enable/disable circuitry, the mode is set by the use of shunts.

The following table shows the PHANTOM configuration header and the proper bank each jumper represents.

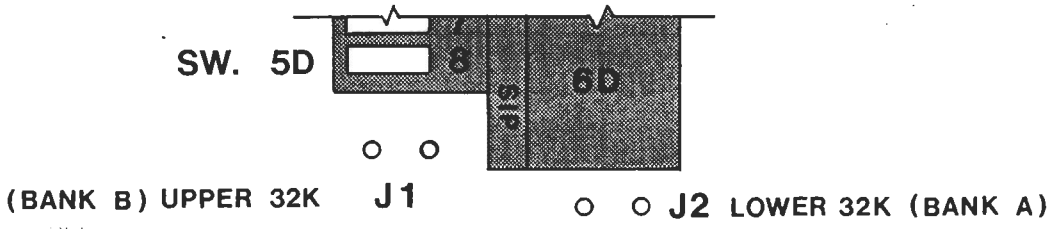


Figure 6-3: PHANTOM CONFIGURATION HEADERS

The following examples indicate the four possible ways that PHANTOM can be set for response.

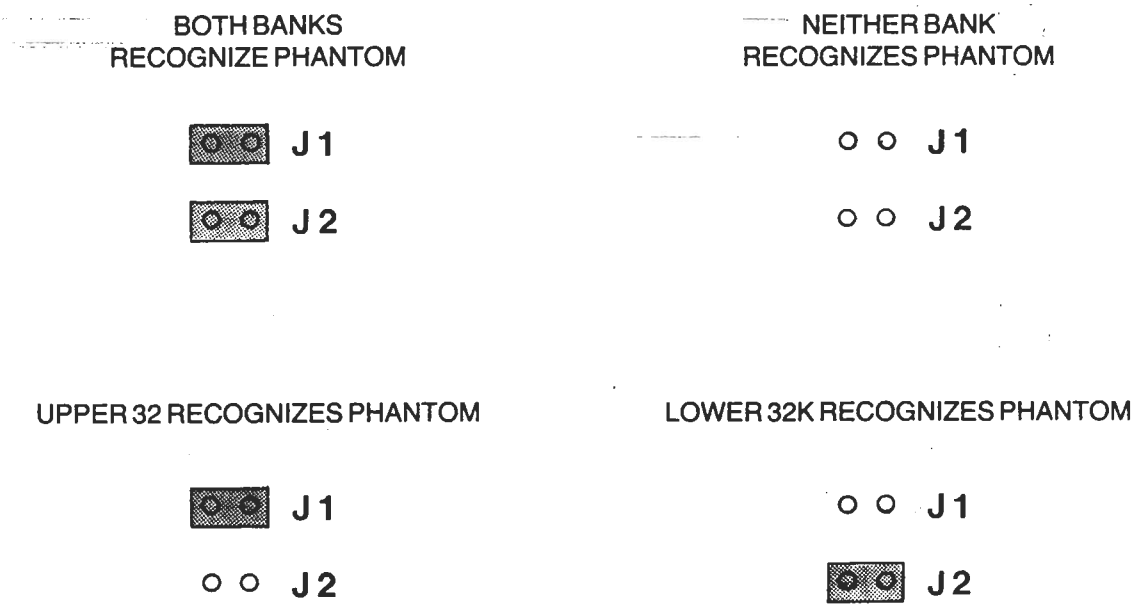


Figure 6-4: PHANTOM CONFIGURATIONS

6.3. MEMORY CONFIGURATION

6.3.1. MEMORY ADDRESSING

The Memory Merchant MM65K16S memory board is configured as four individual 16K blocks of memory. Each of these four blocks can be located on any 16K boundary. Thus, blocks of memory can be assigned at address 0000H, 4000H, 8000H, or C000H.

The DIP switch array located at 5D determines the addressing of the memory board. The DIP switch uses a binary counting system to determine which one of the four blocks will reside on a specific boundary in the memory map.

The table below shows memory addressing:

A15	A14	BLOCK #	ADDRESS FROM–TO	BANK
ON	ON	0	0000H - 3FFFH	A
ON	OFF	1	4000H - 7FFFH	
OFF	ON	2	8000H - BFFFH	B
OFF	OFF	3	C000H - FFFFH	

Table 6-5: MEMORY ADDRESSING TABLE

The table below shows the relationship between the switch settings on the DIP switch at location 5D and the assignment of the individual 16K blocks of memory.

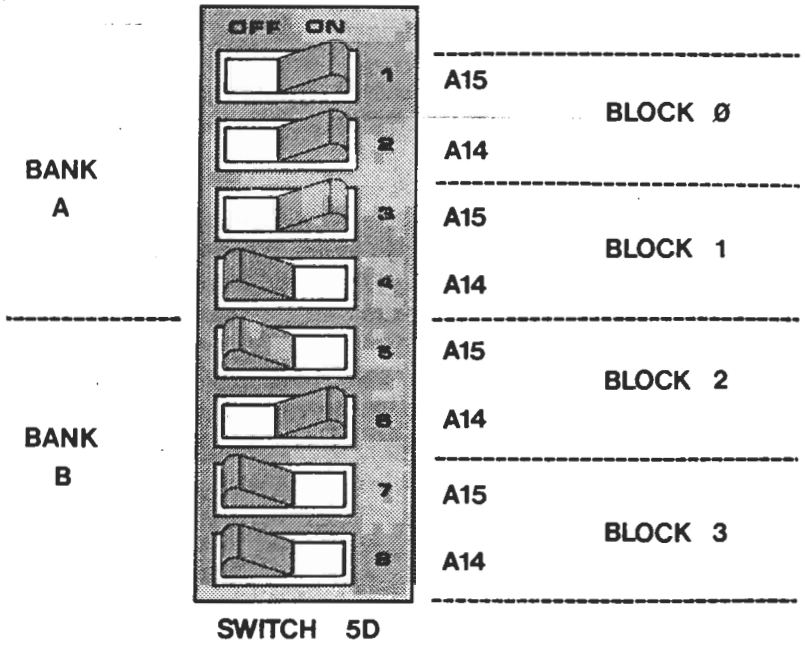
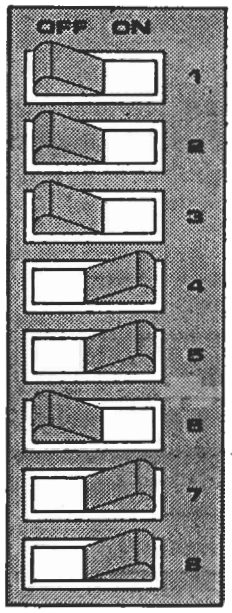


Figure 6-6: ASSIGNMENT OF INDIVIDUAL 16K BLOCKS OF MEMORY

The following examples will show the proper configuration for the memory board so that it will occupy a full 64K compliment.



SWITCH 5D	A15 A14	BLOCK Ø	0000 – 3FFFH
	A15 A14	BLOCK 1	4000 – 7FFFH
	A15 A14	BLOCK 2	8000 – BFFFH
	A15 A14	BLOCK 3	C000 – FFFFH

Figure 6-7: EXAMPLE OF STANDARD 64K CONFIGURATION

6.3.2. 2K SEGMENT DISABLE

The MM65K16S RAM board is capable of disabling a 2K segment of memory anywhere in the memory map. This feature is necessary in systems that might include a memory mapped disk controller or memory mapped video display interface.

The 2K disable feature is assigned to BLOCK 0 (paddle 1 and 2 on switch located at 5D). Because each 16K block can be addressed anywhere within the memory map, if a 2K hole is needed in the memory map were BLOCK 3 is normally addressed, simply reverse the addressing switches and locate BLOCK 3 where BLOCK 0 was addressed and re-address BLOCK 0 to reside where BLOCK 3 was addressed.

A 16-pin header (dual 8) is located between IC 2D and IC 3D and is used to select the 2K segment that is to be removed from the memory map. This header is labeled PAGE 0 at the top of the header and labeled PAGE 7 at the bottom of the header. The PAGE number corresponds to the PAGE in memory that is to be disabled by the placement of a shunt across the header.

The table below shows all possible 2K segment disables:

PAGE	IC	BLOCK 0 (0000–3FFF)	BLOCK 1 (4000–7FFF)	BLOCK 2 (8000–BFFF)	BLOCK 3 (C000–FFFF)
0	3A	0000–07FF	4000–47FF	8000–87FF	C000–C7FF
1	4A	0800–0FFF	4800–4FFF	8800–8FFF	C800–CFFF
2	2B	1000–17FF	5000–57FF	9000–97FF	D000–D7FF
3	2C	1800–1FFF	5800–5FFF	9800–9FFF	D800–DFFF
4	2A	2000–27FF	6000–67FF	A000–A7FF	E000–E7FF
5	1C	2800–2FFF	6800–6FFF	A800–AFFF	E800–EFFF
6	1B	3000–37FF	7000–77FF	B000–B7FF	F000–F7FF
7	1A	3800–3FFF	7800–7FFF	B800–BFFF	F800–FFFF

Table 6-8: 2K SEGMENT DISABLE TABLE

The table above is designed to provide a quick and accurate method of determining the proper location of a 2K segment. For example, if the shunt is placed across PAGE 5 and BLOCK 0 is addressed as BLOCK 0, then memory disabled would be in the address range of 2800 to 2FFF. In the same manner if the shunt was placed across PAGE 7 and BLOCK 0 is addressed as BLOCK 3, then the 2K segment would be disabled from F800 to FFFF.

The following example shows a 2K segment removed at f800 to provide a hole for a memory mapped controller.

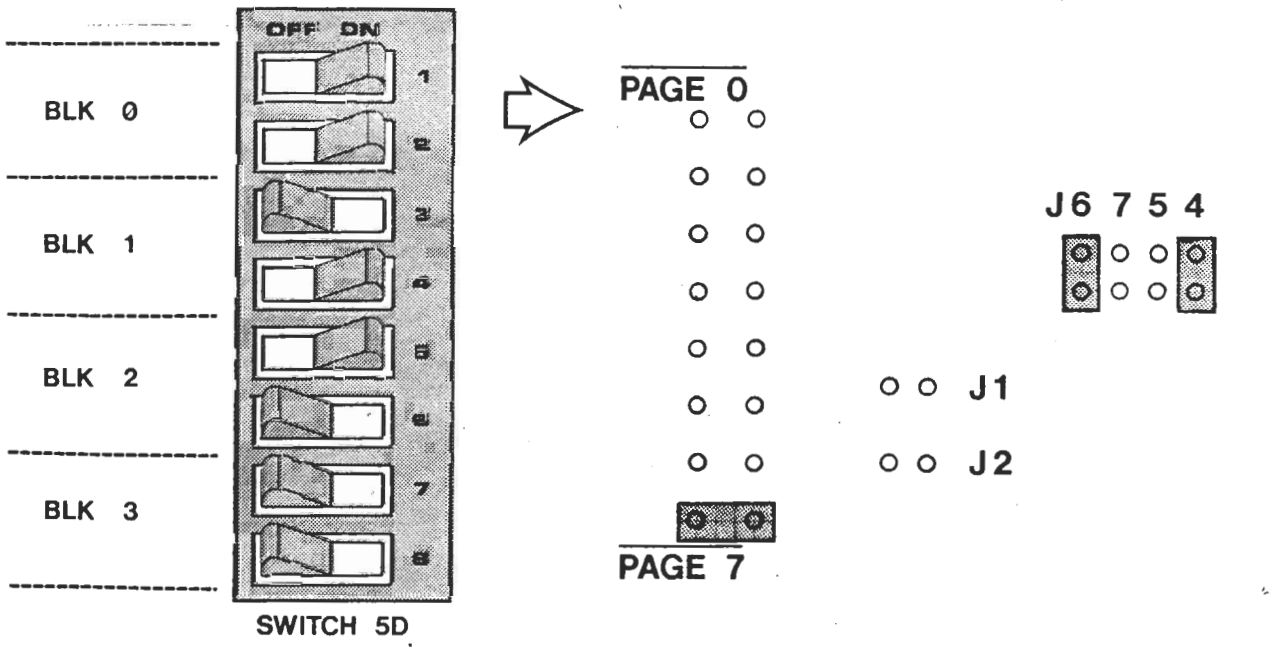


Figure 6-9: EXAMPLE OF 64K CONFIGURATION W/2K REMOVED AT F800

6.3.3. EXTENDED ADDRESSING

The Memory Merchants MM65K16S conforms to the latest IEEE S-100 standard, and can therefore recognize all 24 address lines that are available on the S-100 bus. Use of extended addressing does away with the 64K limitation imposed by most microcomputer systems.

In order for extended addressing to be enabled, location 1D must have a 25LS2521 IC installed. This IC, if not already in location 1D, will probably be found in location 2D (bank select) and should be removed from 2D and reinstalled in location 1D.

Adjacent to the DIP switch 1C is a header labeled J3. This header should NOT have a shunt placed across it unless the board is to be set up for bank select. If there is a shunt placed across J3, it should be removed for proper operation of extended addressing.

Once the 25LS2521 is installed at location 1D and the shunt has been removed from the header at location J3, extended addressing is now activated and bank select has been disabled.

The DIP switch that is located at 1C is used to set the extended addressing for the memory board. By setting the paddles to the OFF position the associated address line is then recognized when it is in its active state.

Extended addressing allows the MM65K16S RAM board to be addressed in 64K increments starting at address 000000H, 010000H, 020000H, up to FF0000H. The DIP switch that is located at 5D then addresses the 64K banks of memory within the extended addressing range. The example below shows the DIP switch at location 1C and its relationship with the incoming address lines.

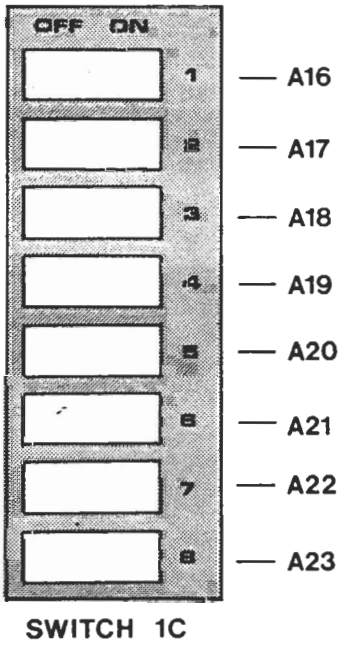


Figure 6-10: DIP SWITCH 1C USED WITH EXTENDED ADDRESSING

The following example indicates the proper switch settings for extended addressing. The board will be set for address 030000H.

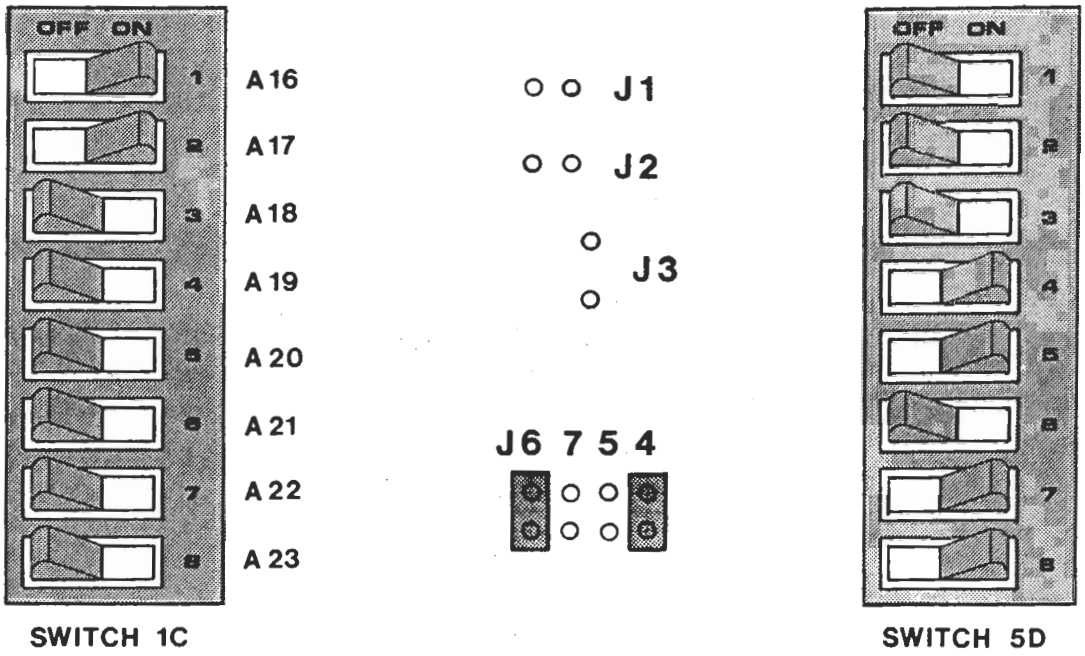


Figure 6-11: EXAMPLE OF EXTENDED ADDRESSING @ 030000H – 03FFFFH

6.3.4. BANK SELECT

For many existing systems designed before the implementation of the IEEE S-100 standard, the use of bank select was mandatory in order to expand memory beyond the 64K limitations. Using a DIP switch and shunt jumpers the MM65K16S RAM board is capable of being configured as any one of 256 I/O ports available, and can enable or disable itself using any one or a combination of the eight data bits available.

In order for bank select to function properly, there must be a 25LS2521 installed in location 2D. If the 25LS2521 is not installed in location 2D, then it will probably be found in location 1D (extended addressing). In any case, it must be installed in location 2D for bank select to function properly.

The next jumper to check is located adjacent to the DIP switch at location 1C on the board. This jumper is labeled J3 and should have a shunt jumper across it. If there is no jumper across J3, one should be installed, otherwise bank select will not function properly.

The third and final check, is the setting of the data bit or bits that will enable or disable the individual banks of memory. There are two headers necessary for configuration. These two headers are located on the lower right hand corner of the board adjacent to IC 16D and are labeled A O and O B at the top of the header blocks and A 7 and 7 B at the bottom of the headers. Bits AO throught A7 control the lower 32K bank of memory and bits OB through 7B control the upper 32K bank of memory.

It is important to remember that all switch settings in the bank select configuration are set to the software that is being used. If the operating system does bank select at port 40H, then the MM65K16S RAM board must be configured to run at port 40H also. The following diagram shows the address lines in relation to the DIP switch at location 1C.

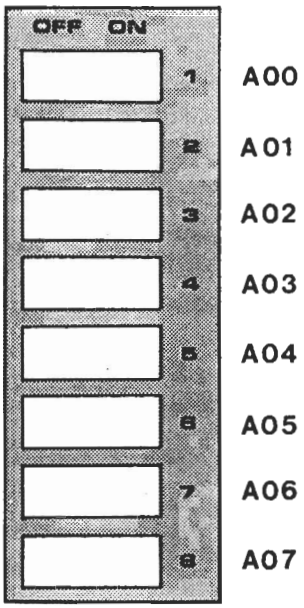


Figure 6-12: DIP SWITCH 1C USED WITH BANK SELECT

In the following diagram the memory board will be configured for port 40H in the bank select mode and data bit-0 will be used to enable both banks of memory.

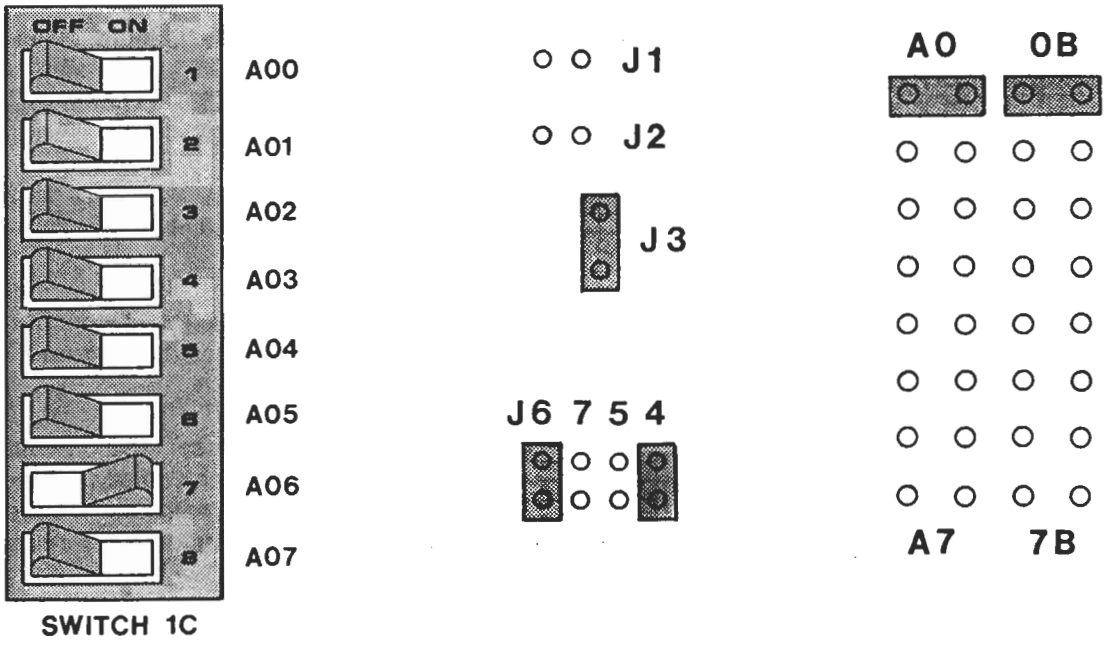


Figure 6-13: EXAMPLE OF BOARD SETUP FOR BANK SELECT

7.1. BOARD PURCHASED AS 48K/32K

The MM65K16S is a 64K Static Ram which is organized as two independent 32K banks. Each 32K bank consists of two blocks of 16K addressable memory. Bank A (lower) has blocks Ø & 1 and bank B (upper) has blocks 2 & 3. Dip switch 5D controls the addressing of these banks. Paddles #1,2,3,4 are tied to blocks Ø & 1 (bank A) and paddles #5,6,7,8 are tied to blocks 2 & 3 (bank B). You must understand that any ENABLED bank or block that does not contain memory chips will cause problems because they are active on the bus. Therefore, an empty bank should be disabled via J7 (bank B) or J5 (bank A). An empty block should be addressed (or switched) the same as the filled block within that same bank.

1.) TABLE SHOWING STANDARD BOARD CONFIGURATION:

BOARD LOADED AS	BANK "A"		BANK "B"	
	BLK Ø	BLK 1	BLK 2	BLK 3
32K	16K	16K	—	—
48K	16K	16K	16K	—
64K	16K	16K	16K	16K

PURCHASED AS A 32K:

When purchasing the memory board with only 32K of memory, it must be noted that all 32K is contained in bank "A" - blocks Ø and 1. If two independent 16K banks are required rather than one 32K bank, this can be accomplished by removing the 8 memory chips located in block 1 and re-inserted into block 2 of bank "B". (see table 2.)

PURCHASED AS A 48K:

When purchasing the memory board with only 48K of memory, it must be noted that 32K is contained in bank "A" - blocks Ø and 1 and 16K is contained in bank "B" - block 2. (block 3 is empty) If you want all 48K of memory to reside in just one bank, then you would have to purchase our option #A48/16 (PAL14L4) which would change bank "A" to 48K and bank "B" to 16K. This option was designed to enable the MM65K16S to work with MP/M.

2.) TABLE SHOWING PHYSICAL LOCATION OF RAM CHIPS IN BLOCKS Ø THRU 3:

BLOCK Ø*	1A	1B	1C	2A	2B	2C	3A	4A
BLOCK 1	3B	3C	4B	4C	5A	5B	5C	6A
BLOCK 2	6B	7A	7B	7C	8A	8B	8C	9A
BLOCK 3	9B	9C	10A	10B	10C	11A	11B	11C

*BLOCK Ø HAS THE 2K SEGMENT DISABLE FEATURE (SW. 5D - PADDLES #1,2)

7.1.1 OPTION #A48/16

The Model MM65K16S is a very versatile memory board. Flexibility was designed-in to customize the board at a later date via the use of sofisticated programmed on-board logic chips. The board uses one FPLA (82S100) and two PAL's (14L4 and 16L2). Our first option is the #A48/16 which changes the two independent 32K banks to one 48K bank "A" and one 16K bank "B" for use in MP/M software.

To use this option, simply remove (carefully) the standard PAL14L4 which can be found at IC location 6D and insert (observing polarity) the #A48/16 (new PAL14L4) into that same socket (6D). You must remember that bank "A" now consists of blocks Ø,1,2 and bank "B" has block 3. The memory addressing switch (5D) paddles #1,2,3,4,5,6 are now tied to the "J2" phantom line and J5,4 enable/disable lines.

1.) TABLE SHOWING STANDARD BOARD CONFIGURATION:

BOARD LOADED AS	BANK "A"		BANK "B"	
	BLK Ø	BLK 1	BLK 2	BLK 3
32K	16K	16K	—	—
48K	16K	16K	16K	—
64K	16K	16K	16K	16K

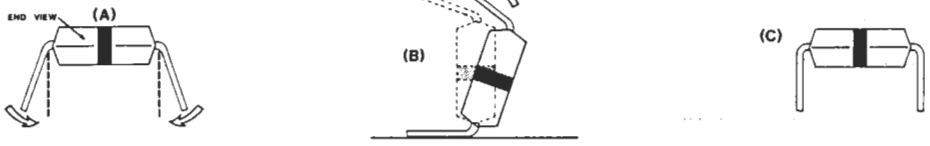
2.) TABLE SHOWING CONFIGURATION WITH OPTION #A48/16 INSTALLED (6D):

BOARD LOADED AS	BANK "A"			BANK "B"
	BLK Ø	BLK 1	BLK 2	BLK 3
32K	16K	16K	—	—
48K	16K	16K	16K	—
64K	16K	16K	16K	16K

7.2 REMOVING/INSERTING IC'S

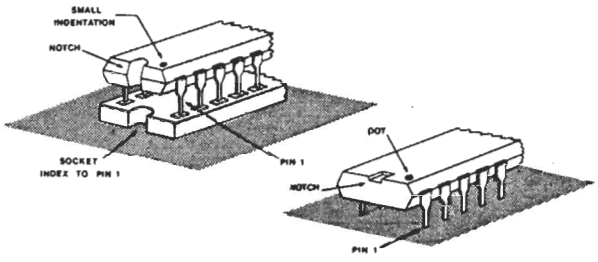
Because of the versatile nature of the MM65K16S memory board, it may be necessary to remove or insert rams, eproms or optional integrated circuits. Before proceeding with any of these changes, it is important that you read the following.

The pins on most of the IC's manufactured are normally bent out at an angle (see- "A"), so they do not line up with the holes in the IC sockets. DO NOT try to install an IC without first bending the pins as described below. Doing so may damage the pins on the IC and/or the contacts in the socket - causing intermittent contact. Before you install the IC, lay it down on its side as shown below (see - "B") and very carefully roll it toward the pins to bend the lower pins into line. Then turn the IC over and bend the pins on the other side in the same manner. If the IC has a ceramic body, be especially careful bending the leads as ceramic bodies have a tendency to chip and thereby causing damage to that IC. The finished product should appear as shown in "C". A preferred technique for insertion or removal would be to use a tool especially designed for that purpose. We use some excellent tools made by the Erem Corporation. Tool #505A is for 24/28 pin with .600 lead spacing - #505J for 18/20 pin with .300 lead spacing and #505C for 14/16 pin with .300 LS. These are very high quality tools and can be located at distributors specializing in electronic tools. If you need any help, feel free to call or write to us for information.



POLARITY

It is extremely important that the IC'S being inserted into the IC sockets are positioned for correct polarity. Inserting the IC backwards can cause immediate damage to that IC. This will also cause one of the voltage regulators to exhibit a very low voltage which will render the memory board inoperable. Below are diagrams for correct positioning of the IC'S.



7.3. USING EPROMS/ BIPOLAR PROMS (5V)

EPROMS

When using a programmed 2716 (5V) EPROM, it is necessary to remember that the MM65K16S memory board DOES NOT generate any type of wait states for the processor. Therefore, it is mandatory that the EPROMS being used are fast enough. If a 4 Mhz processor is being used, then the EPROM must have an access time of 300ns (max.) or faster. Using a slower EPROM is almost a certain guarantee of problems. Since we are not aware of any manufacturer that produces a 2716 faster than 350ns (max.), we suggest that you consider using a BIPOLAR PROM if speed is critical. Below, we have listed 3 manufacturers of 2716's which have the fastest access times available at this time. Remember that these are "Max. Speeds" - Typical access times may actually be fast enough for your system. Some manufacturers are very conservative on their spec. sheets. Fujitsu America is one such manufacturer. Their part has been known to run close to 200ns although the max. spec. is rated @ 350ns. Even though we cannot guarantee that they will run at this speed, it might be worth a try.

EPROMS: (5V)

MFG.	PART NO.	(max.) Access Time
FUJITSU	MBM2716H	350ns
INTEL	C2716-1	350ns
MOTOROLA	MCM2716C35	350ns

BIPOLAR PROMS

The BIPOLAR PROM equivalent is a fusable link part that can be programmed ONLY ONCE, but is available with access times that will guarantee speeds in excess of 6 Mhz. While they solve the speed problems, be aware that they are more expensive than EPROMS, and you can program these parts ONLY ONCE! For your convenience, we have listed 5 manufacturers of BIPOLAR PROMS.

BIPOLAR PROMS:

MFG.	PART NO.	(max.) Access Time	ICC Power @ 5V
INTEL	3636	65ns	150ma TYP./185ma. max.
NEC	UPB429	70ns	100ma TYP./160ma. max.
FUJITSU	MB7138E	55ns	130ma TYP./180ma. max.
HARRIS	HM76161-5	60ns	N/A /180ma. max.
SIGNETICS	N82S191	80ns	130ma TYP./175ma. max.

PLEASE NOTE

BIPOLAR PROMS use considerably more current than EPROMS and you must be careful NOT TO EXCEED the available regulation provided on the MM65K16S memory board. Also, each manufacturer's programming specifications differ from each other. Please consult your nearest distributor/factory representative for current information on specs., prices, availability and programming services in your area. If you need additional help, please call or write to us and we will try and assist you.

7.4. MULTIPLE BANK CONTROL FEATURE

One of the more interesting features of the MM65K16S is the manner in which the bank select feature operates. The MM65K16S allows for a total of eight independent users, but by using multiple data bits, one bank of memory can be "forced" to follow other banks of memory, or one board could control multiple banks of memory.

The example below is an example of how the multiple bank feature functions. The data bits for A0 to A7 are set up to represent a data pattern of 83H. Data bits 0B to B7 are set up to represent a data pattern of 03H.

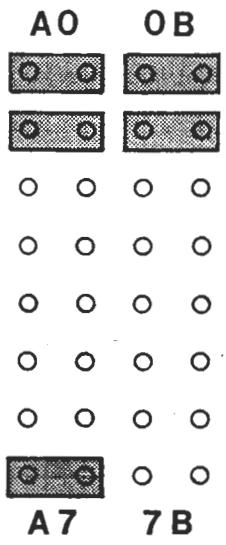


Figure 7-4: EXAMPLE OF MULTIPLE BANK CONTROL

In the above example, data bits 0 and 1 were enabled on both the upper and lower banks of memory. The lower bank of memory had data bit-7 set also, and this should be noted.

Whenever the system software issues a bank select command and the data that is sent to the board is equal to the strapping of the data bits, the board will then enable or disable.

The upper bank of memory will respond to data that is equal to 03H (bits 0 and 1), but it will also respond to ANY data pattern that has data bits 0 and 1 set. In other words, this Bank will respond to data patterns of 03H, 07H, 83H, 13H, 4BH, 6FH etc. With this in mind, it is possible for the system software to issue one bank select command and control multiple banks of memory.

The lower bank of memory, (remember data bit-07 was set) is set to recognize a data pattern of 83H, but will respond to any data that has bits 0,1, and 7 set. So, the lower bank of memory could be set to enable or disable when the system software issues a bank select command and the data patterns are 93H, A3H, F3H, or B7H. Therefore, this bank responds to the system commands in the same fashion as the upper bank responded.

7.5. INSTRUCTIONS FOR CROMIX* USE

The MM65K16S memory board can be configured to meet the blank and addressing requirements of a Cromemco Cromix system. To use the MM65K16S memory as one of the memory boards in the Cromix system, it is mandatory that each of the 32K banks are completely populated.

Although Cromix requires 64K banks to operate, this memory must exist as two (2) separate 32K banks both of which must be independently selectable. This feature of independent selection allows the operating system to load a small overhead program in the upper bank-B of all memory boards in the system. To accomplish this requirement, the upper bank-B of each memory board must respond to a high in bit 7 output to port 40 hex.

The MM65K16S memory board can be configured either as the system bank or as any one of the 6 user banks. There is only one board configured as the system bank at any one time, but there maybe one or more user banks in the system.

CONFIGURING THE MM65K16S AS THE SYSTEM BANK

The system memory bank must be jumpered to have the lower 32K bank-A enabled and the upper 32-K bank-B disabled on power up or reset. Jumper J4 and J7 should be installed to provide the necessary banks.

The system memory bank must have both 32K banks respond to all bits of an output to port 40 hex except those bits which are defined as user banks. The system bank memory board must respond to bit 0 and bit 7. Data bit 0 is the unique bit for the system bank and data bit 7 is the bit that all memory boards must respond to. The remaining data bits starting with data bit 1 are designated as user bank selection bits. The system bank must also be jumpered to all unused bank bits.

EXAMPLE: SINGLE USER SYSTEM

In a single user system there is only one system bank and one user bank. The system bank must be jumpered to respond to data bits 0, 2, 3, 4, 5, 6 and 7. Data bit 1 is reserved as the user bank 1.

EXAMPLE: MULTIPLE USER SYSTEM

In a two user system there is only one system bank but there are two user banks. The system bank must be jumpered to respond to data bits 0, 3, 4, 5, 6 and 7. Data bits 1 and 2 are reserved as user banks 1 and 2 respectfully.

CONFIGURING THE MM65K16S AS USER BANKS

All memory boards which are designated as user banks must be jumpered to be deselected on power up or reset. This is accomplished by jumpers J5 and J7. The two 32K banks on each user bank boards must respond slightly different than from each other. The lower 32K bank-A must be jumpered to respond to only the data bit corresponding to that user bank, ie., data bit 1 as user bank 1 or data bit 2 as user bank 2 or data bit 3 as user bank 3. The upper 32K bank-B must also respond to the same data bit as the lower 32K bank-A on that memory board as well as it must respond to data bit 7.

NOTE: All upper 32K banks on all user banks must respond to data bit 7 as well as the data bit corresponding to the user bank number.

EXAMPLE: USER BANK 1

Jumper data bit 1 in both the lower-A and upper-B 32K banks. Jumper data bit 7 in the upper 32K bank-B also.

EXAMPLE: USER BANK 2

Jumper data bit 2 in both the lower-A and upper-B 32K banks. Jumper data bit 7 in the upper 32K bank-B also.

FEATURES COMMON TO ALL MEMORY BOARDS

1. No bank on any memory board used in the Cromix system should be jumpered to respond to the PHANTOM line.

2. The memory should be configured to provide a contiguous 64K of memory. This is done by assigning the 4 board addresses to 0000H, 4000H, 8000H, and C000H. (as shown on page 10)

3. The bank select port must be assigned to port 40 hex. (shown on pg. 14)

8. IF YOUR BOARD FAILS TO OPERATE!

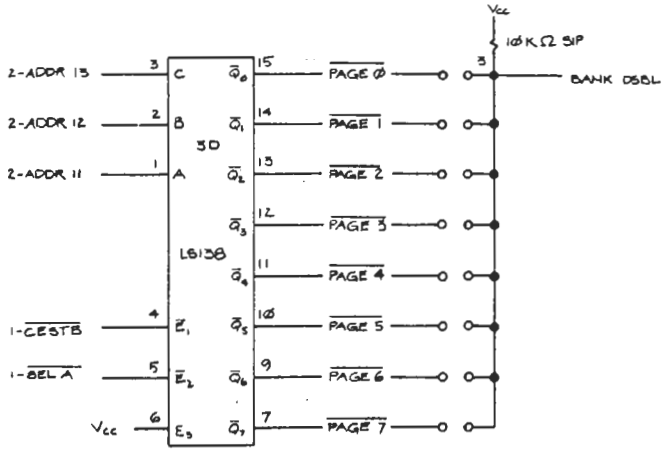
Memory Merchant puts every board through rigorous testing procedures to insure that our boards do not fail in the field. But problems to occur. The three main reasons are:

A.) The memory board is not configured correctly for the system it is being used in...
B.) Incompatibility with other products that do not fully conform to all current IEEE 696/S-100 standards.
C.) Actual memory board failure.

NOTE A.) Please understand that the board, as shipped from the factory, is not ready to be put into any system until it is configured correctly. If you failed to read pg. 6 "How the board is shipped" and section "6. Installation Procedures" - please go back and do so. Some possible problems: failure to place a shunt on header "J3" and making sure that all shunts, that are installed, are connecting BOTH PINS. Placing a shunt on the wrong Phantom line for the address used on dip switch 5D. Not fully understanding Dip switch 5D (paddles #1,2) - Block Ø for proper 2K segment disable.

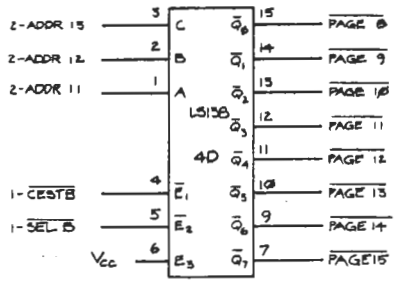
NOTE B.) The S-100 bus has standards that were meant to be followed. Some manufacturers do not, although they claim to, fully conform to the latest IEEE 696/standards. All Memory Merchant S-100 products conform to those standards in every respect. Our memory boards are fully compatible with such manufacturers as: Cromemco, Northstar, Morrow Designs, Compupro (Godbout Electronics), Vector Graphics and many others. If you are certain the board is configured correctly, then I suggest you check the other manufacturer's schematics on their CPU or disk controller boards and make sure that they are generating all the control signals required for proper operation of the S-100 bus.

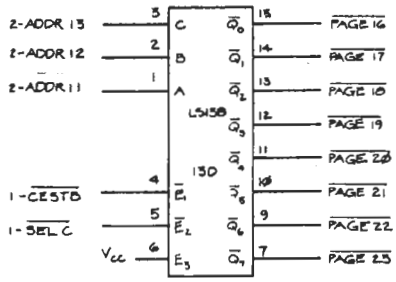
NOTE C.) If notes A & B have been checked and everything appears to be in order, then it is possible the memory board itself has failed to function properly. Please read pg. 3 and call or write for a Return Authorization Number.

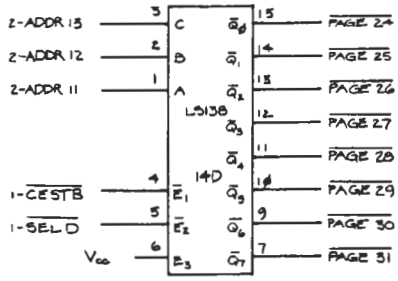


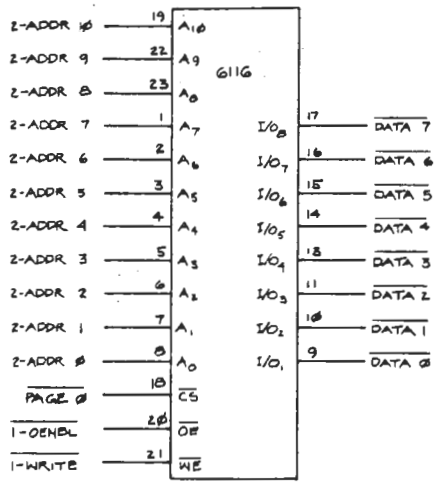
PAGE Ø - 3A	PAGE 16 - 7A
PAGE 1 - 4A	PAGE 17 - 8A
PAGE 2 - 2B	PAGE 18 - 9A
PAGE 3 - 2C	PAGE 19 - 6B
PAGE 4 - 2A	PAGE 20 - 8B
PAGE 5 - 1C	PAGE 21 - 7B
PAGE 6 - 1B	PAGE 22 - 7C
PAGE 7 - 1A	PAGE 23 - 8C
PAGE 8 - 4B	PAGE 24 - 11A
PAGE 9 - 5D	PAGE 25 - 11B
PAGE 10 - 4C	PAGE 26 - 11C
PAGE 11 - 5C	PAGE 27 - 10C
PAGE 12 - 3C	PAGE 28 - 10B
PAGE 13 - 6A	PAGE 29 - 10A
PAGE 14 - 3B	PAGE 30 - 9C
PAGE 15 - 5A	PAGE 31 - 9B

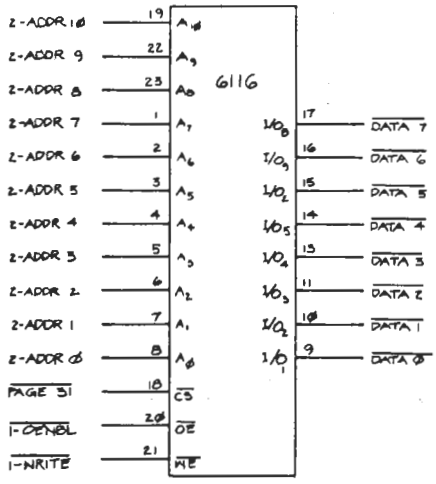
PHYSICAL LAYOUT OF LOGICAL MEMORY PAGES











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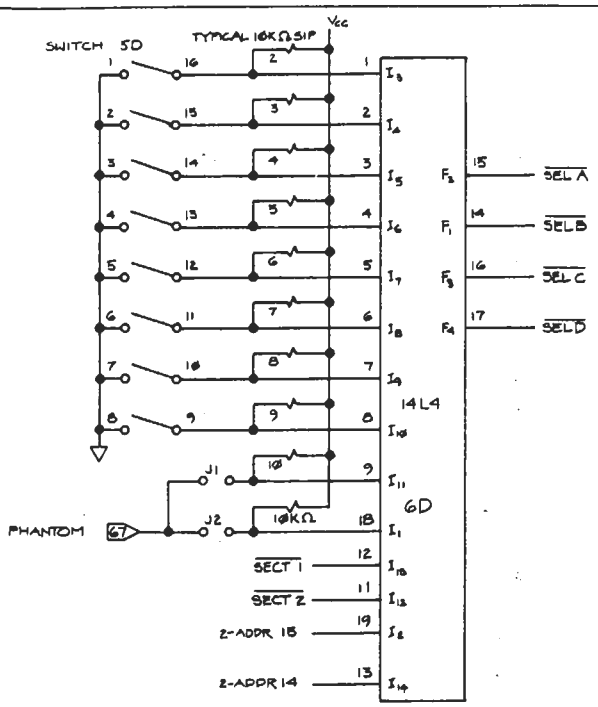

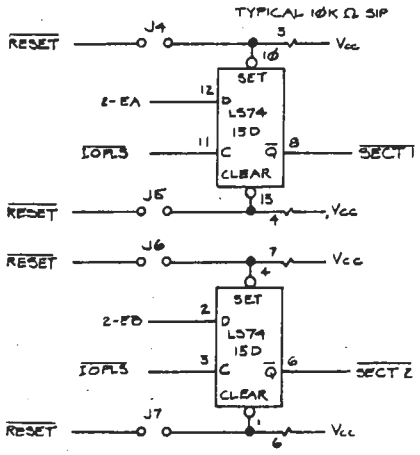

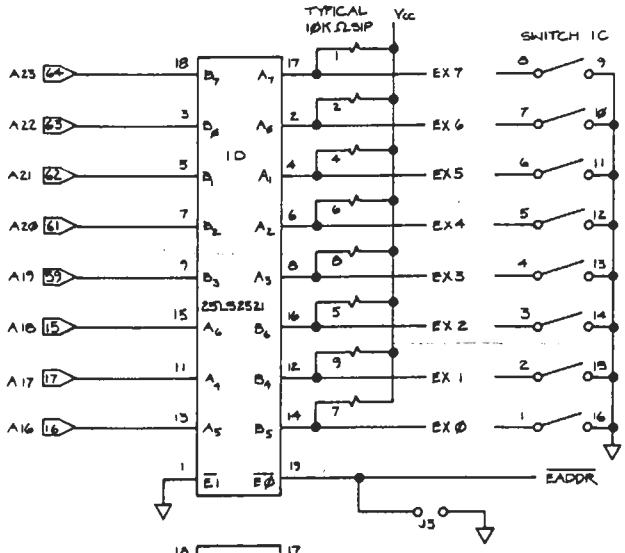

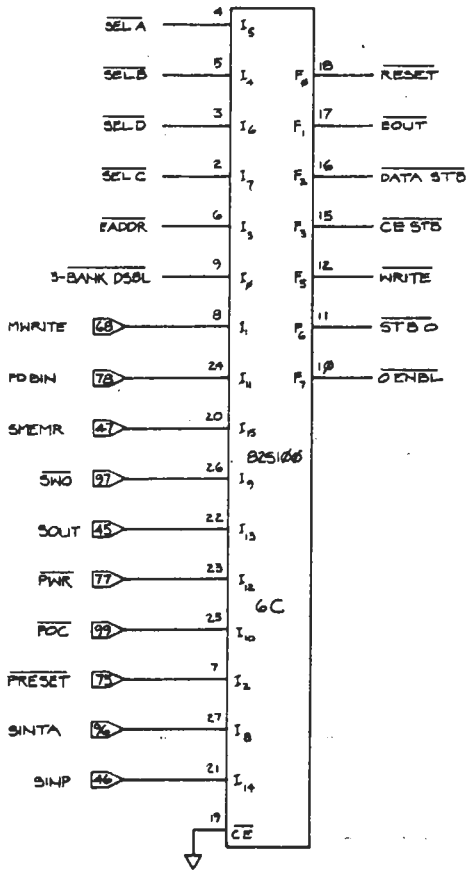

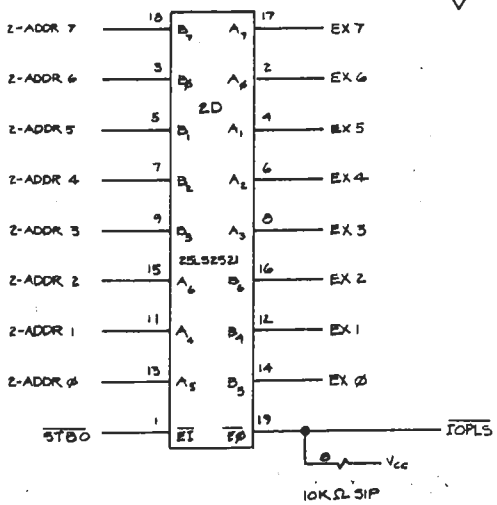

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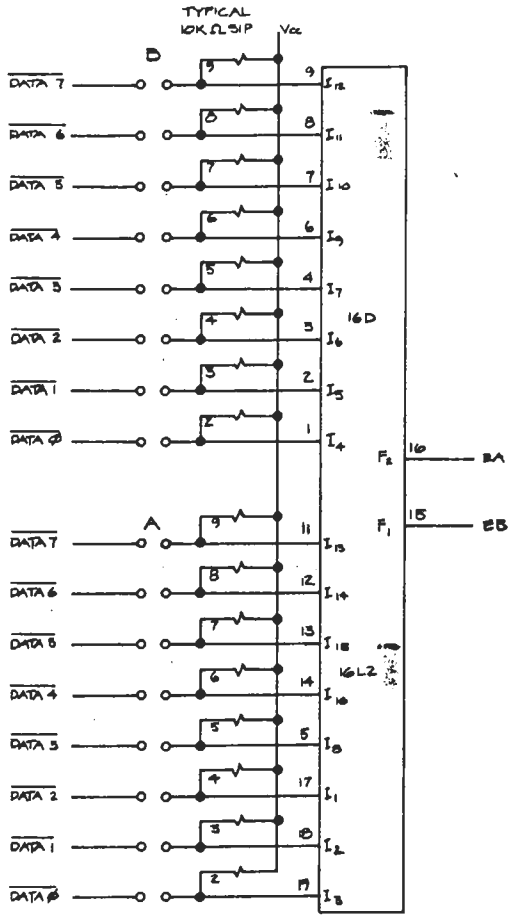
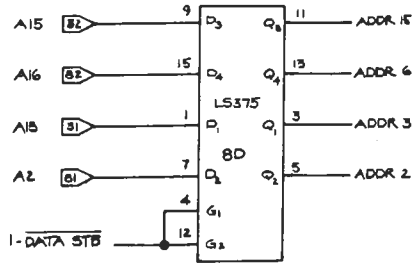
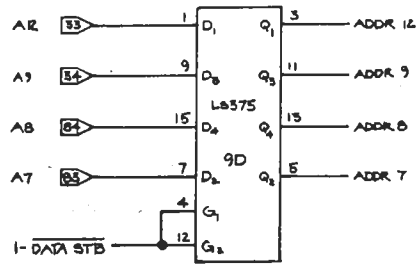
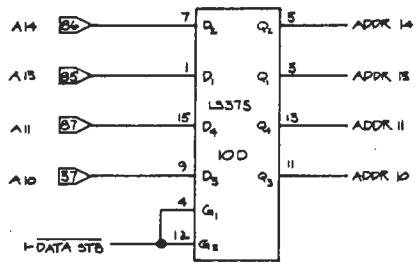
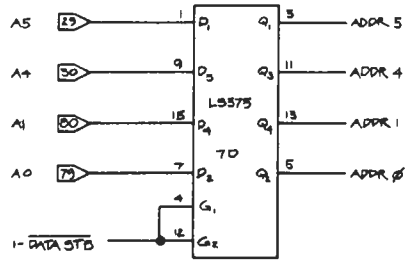
		DATE: 11/81

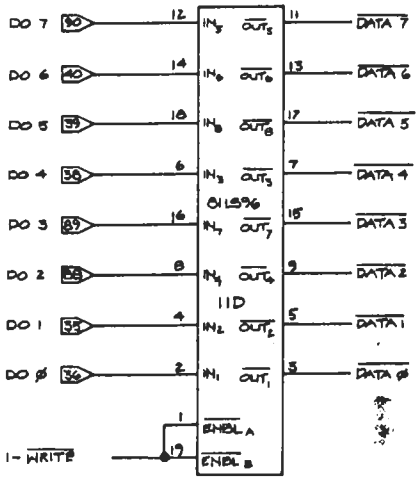


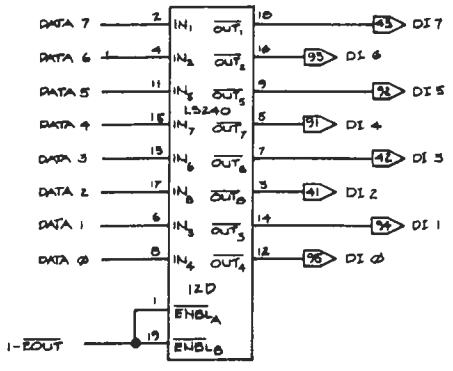












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